REMARKS

In response to the Office Action dated October 25, 2010 Applicant respectfully requests reconsideration based on the above claim amendments and the following remarks. Applicant respectfully submits that the claims as presented are in condition for allowance.

Claims 1-11 and 14-17 are pending in the present Application. Claims 1 and 7 are amended, and Claim 17 is cancelled, leaving Claims 1-11 and 14-16 for consideration upon entry of the present amendments and the following remarks.

Support for the claim amendments is at least found in the specification, the figures, and the claims as originally filed. Particularly, support for amended Claims 1 and 7 is at least found in originally filed Figure 4, and in the specification at page 8, line 17 to page 9, line 4, and page 9, lines 10-17.

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

Claim Rejections under 35 U.S.C. §103

For an obviousness rejection to be proper, the Examiner is expected to meet the burden of establishing why the differences between the prior art and that claimed would have been obvious. (MPEP 2141(III)) "A patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.,* 127 S.Ct. 1727, 1741 (2007). To find obviousness, the Examiner must "identify a reason that would have prompted a person of ordinary skill in the art in the relevant field to combine the elements in the way the claimed new invention does." *Id.* Also, to establish *prima facie* obviousness of a claimed invention, the prior art references must teach or suggest all of the claim limitations. (MPEP 2143(A)(1))

Claims **1**, 2, 4-6, 15-17 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Katagawa, U.S. Patent No. 7,079,105 (hereinafter "Katagawa") in view of in view of Nakamura et al., U.S. Patent No. 7,136,058 (hereinafter "Nakamura").

Claims 3, **7**-11 and 14 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Katagawa in view of Nakamura, and further in view of Kawaguchi et al., U.S. Patent No. 5,592,199 (hereinafter "Kawaguchi").

Applicant respectfully traverses the rejections for the reasons set forth below. Applicant respectfully notes that Claim 17 is hereinabove cancelled without prejudice.

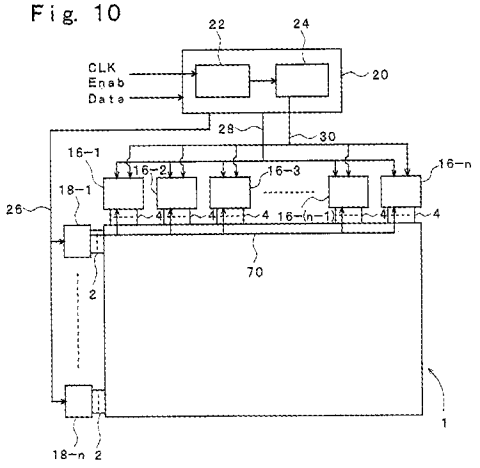
Amended independent **Claims 1 and 7** similarly recite, *inter alia*:

> "An LCD apparatus comprising:
> an LCD panel displaying images and including *an output instruction signal line disposed on the second substrate and opposing the common electrode*;
> *a data driver disposed on a data tape carrier package (TCP);*
> a gate driver outputting a gate driving signal to the LCD panel; and
> *a timing controller on a printed circuit board*, the timing controller providing a first control signal to the gate driver so as to control an output of the gate driving signal, and providing an output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load solely defined by the output instruction signal line opposing the common electrode, and depending on a resistive load of the output instruction signal line,
> *wherein the output instruction signal line is disposed between the data TCP and the gate lines, and is connected to the timing controller through the data TCP.*"

Regarding **Katagawa** in the instant Office action at Pages 2, 3 and 7-9, it is asserted that latch pulse supply line 70 in Figure 10 (reproduced below) teaches the "output instruction signal line" between data driver 16-1 (as a "data TCP") and gate bus 2 (as the "gate lines").

Katagawa teaches the latch pulse supply line 70 is extracted from gate driver 18-1 and is provided above the gate bus 2, where branch lines in the middle of the latch pulse line 70 are wired to the data drivers 16-1 to 16-n. (See, Col. 11, lines 41-57, Col. 12, lines 24-36 (reproduced below) and Figure 10 of Katagawa.) Katagawa further teaches that latch pulses of the TFT-LCD 1 are output from timing controller 20 to the latch pulse supply line 70 through the gate driver 18-1 and control line 26. (*Id.*) That is, the latch pulse line 70 (as the "output instruction signal line") of Katagawa is connected to a timing controller 20 through the gate driver 18-1, and is not connected to the timing controller 20 through the *data driver 16-1* (as the "data TCP").

Fig. 10



Therefore, Katagawa *does not teach or suggest* **a data driver disposed on a data tape carrier package (TCP), a timing controller on a printed circuit board**, the timing controller

providing a first control signal to the gate driver so as to control an output of the gate driving signal, and providing an output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load solely defined by the output instruction signal line opposing the common electrode, and depending on a resistive load of the output instruction signal line, **wherein *the output instruction signal line is* disposed between the data TCP and the gate lines, and is *connected to the timing controller through the data TCP*** of similarly amended independent Claims 1 and 7.

It is conceded that Katagawa 1) is silent as to the source of the capacitive load delay on the instruction signal line, and 2) does not expressly disclose that the output instructions signal line is disposed opposite the common electrode.

Regarding **Nakamura** in the instant Office action with respect to independent Claims 1 and 7 at Pages 4, 5, 9 and 10, Nakamura is relied upon as allegedly teaching a common electrode disposed on the first substrate and opposing a "signal line." Specifically, Col. 4, lines 10-19, *power supply* wiring pattern P1 and *capacitor* elements C4,C5 wiring in Figures 14 and 15 of Nakamura are relied upon as teaching "signal lines" disposed on the second substrate and opposing the common electrode.

Nakamura teaches signal lines through which an amplified and D/A converted analog *video signal* passes. (See, for example, Col. 4, lines 10-11 and 21-24.) Nakamura teaches *power supply wiring* pattern P1 of AMP 17 which amplifies an output from the DAC 16, overlaps common electrode 23. (See, Col. 15, lines 43-48.) Nakamura further teaches *capacitor* elements C4 and C5 are connected between stages of inverters IV1 to IV 3 *in the AMP 17*. (See, Col. 15, lines 51-55 and Figure 15.)

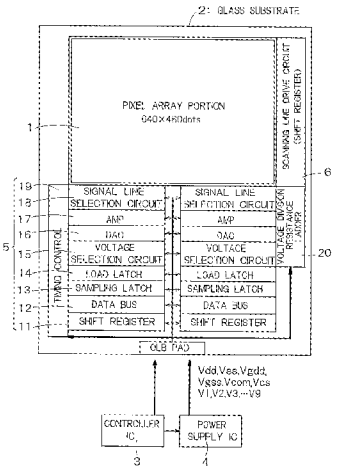
Referring to Figure 1 (reproduced below) of Nakamura, elements from the signal line selection circuit 18 to the shift register 11 are considered as a "data driver" which integrated on a substrate and including P1, C4 and C5. Arrowhead lines between the controller IC3 and power supply IC 4, and the glass substrate 2 are a connection of a controller and the "data driver."

That is, the lines of Nakamura are power supply lines for an AMP (See FIG. 14) or capacitors of the AMP (See FIG. 15), which consist of *a data driver* integrated on a substrate (See FIG. 1), such that the lines of Nakamura do not teach at least "providing an output instruction signal to the data driver *via the output instruction signal line*," and are not "disposed

between the data driver and the gate lines" nor "connected to the timing controller *through the data driver*."

FIG. **1** is a block diagram showing a schematic structure of a first embodiment of a display apparatus according to the present invention and illustrates a block structure of a liquid crystal display apparatus. The liquid crystal display apparatus depicted in FIG. **1** includes a glass substrate **2** in which a pixel array portion **1** and drive circuits are integrally formed. The glass substrate **2** is arranged so as to be opposed to a non-illustrated opposed substrate and sealed with a liquid crystal layer therebetween.

As separate from the glass substrate **2** illustrated in FIG. **1**, there is provided a substrate having mounted thereon a controller IC**3** which transmits a digital video signal and a control signal to the drive circuit and a power supply IC**4** which supplies a power supply voltage, and these substrates are connected to each other through a flexible printed board or the like.



Therefore, Nakamura *does not teach or suggest* **a data driver disposed on a data tape carrier package (TCP), a timing controller on a printed circuit board**, the timing controller providing a first control signal to the gate driver so as to control an output of the gate driving signal, and providing an output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load solely defined by the output instruction signal line opposing the common electrode, and depending on a resistive load of the output instruction signal line, **wherein *the output instruction signal line is* disposed between the data TCP and the gate lines, and is *connected to the timing controller through the data TCP*** of similarly amended independent Claims 1 and 7, and does not remedy the deficiencies of Katagawa noted above.

Furthermore, since P1, C4 and C5 of Nakamura are functionally different from the signal line of Katagawa transferring a latch signal, and since Katagawa is silent as to the source of the capacitive load delay on the instruction signal line and does not expressly disclose that the output instructions signal line is disposed opposite the common electrode, Applicants respectfully submit that there exists *no suggestion or motivation* to modify or combine at least Katagawa and Nakamura to teach **a data driver disposed on a data tape carrier package (TCP), a timing controller on a printed circuit board**, providing a first control signal to the gate driver so as to control an output of the gate driving signal, **and providing an output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load solely defined by the output instruction signal line opposing**

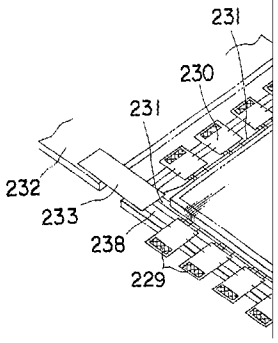
the common electrode, and **depending on a resistive load of the output instruction signal line, wherein *the output instruction signal line is* disposed between the data TCP and the gate lines, and is *connected to the timing controller through the data TCP*** of similarly amended independent Claims 1 and 7.

It is conceded that the combination of Katagawa and Nakamura does not expressly disclose a plurality of signal transmission members.

Regarding **Kawaguchi** in the instant Office action at Pages 7, 10 and 11, common lines 231 and output terminal 246/electrode terminal 248 in Figure 32 are respectively considered as teaching the "output instruction signal line" and a "signal transmission member" of the claimed invention. It is asserted that the common lines 231 receives the "output instruction signal" from a "timing controller" (connector 8/control board 232 in previous Office actions) via one of the output terminal 246/electrode terminal 248 (as "signal transmission member"), noting the connection of common lines 231 with connecting portion 240/lead lines 242 in Figure 32.

As discussed above, common lines 231 of Kawaguchi are considered as teaching the "output instruction signal line." Referring to Figure 30 (portion reproduced below) of Kawaguchi, the common lines 231 are not connected to the connector 8/control board 232 (as a "timing controller") through the flexible wiring boards 230 along y-axis with six drive IC's 229 (as a "data TCP"). Therefore, Kawaguchi *does not teach or suggest* at least **a data driver disposed on a data tape carrier package (TCP), a timing controller on a printed circuit board, wherein *the output instruction signal line is* disposed between the data TCP and the gate lines, and is *connected to the timing controller through the data TCP*** of similarly amended independent Claims 1 and 7, and does not remedy the deficiencies of Katagawa and Nakamura noted above.

Fig. 30



Thus, since Katagawa, Nakamura and Kawaguchi, alone or in combination, *fail to teach or suggest all of the limitations* of similarly amended independent Claims 1 and 7, *prima facie* obviousness does not exist regarding at least amended independent Claims 1 and 7 with respect to Katagawa, Nakamura and Kawaguchi. Applicant respectfully submits that Claims 1 and 7,

and Claims 2-6, 8-11 and 14-16 as respectively depending from Claims 1 and 7, are not further rejected or objected, and are therefore allowable. Entry of the claim amendments, reconsideration, withdrawal of the relevant §103 rejections and allowance of Claims 1-11 and 14-16 are respectfully requested.

Conclusion

All of the objections and rejections are herein overcome. In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. No new matter is added by way of the present Amendments and Remarks, as support is found throughout the original filed specification, claims and drawings. Prompt issuance of Notice of Allowance is respectfully requested.

The Examiner is invited to contact Applicant's attorney at the below listed phone number regarding this response or otherwise concerning the present application.

Applicant hereby petitions for any necessary extension of time required under 37 C.F.R. 1.136(a) or 1.136(b) which may be required for entry and consideration of the present Reply.

If there are any charges due with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicant's attorneys.

Respectfully submitted,

CANTOR COLBURN LLP

By: /Amy Bizon-Copp/

Amy Bizon-Copp
Registration No. 53,993
CANTOR COLBURN LLP
20 Church Street
22nd Floor
Hartford, CT 06103
Telephone (860) 286-2929
Facsimile (860) 286-0115
Customer No. 23413

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